Low Mass, High Speed Silicon Tracking

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Project X Workshop

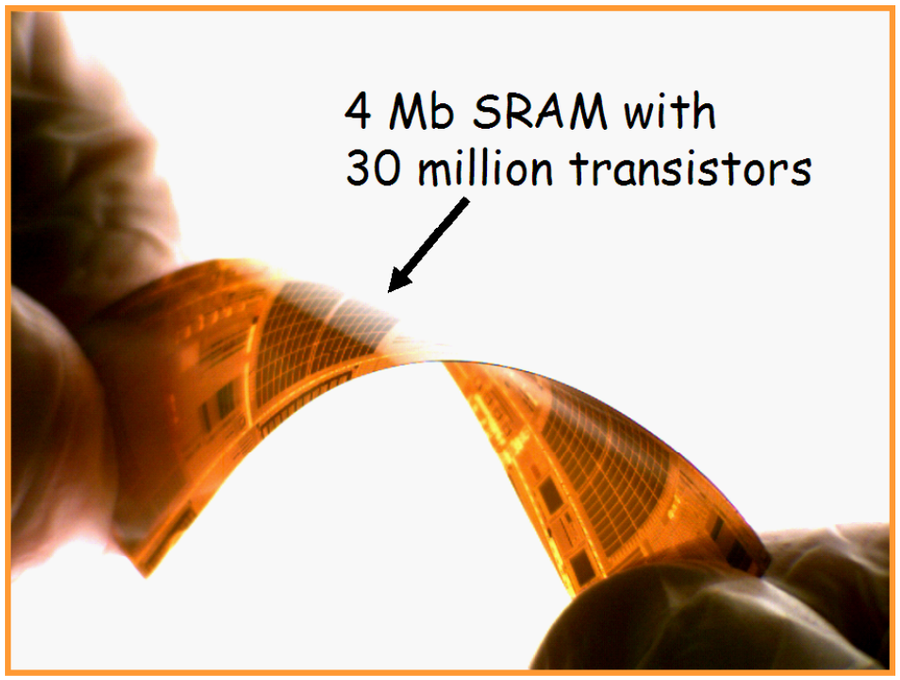
Some Principles

Thinned sensors

Power consumption

Speed tradeoffs

Conclusions and Prospects



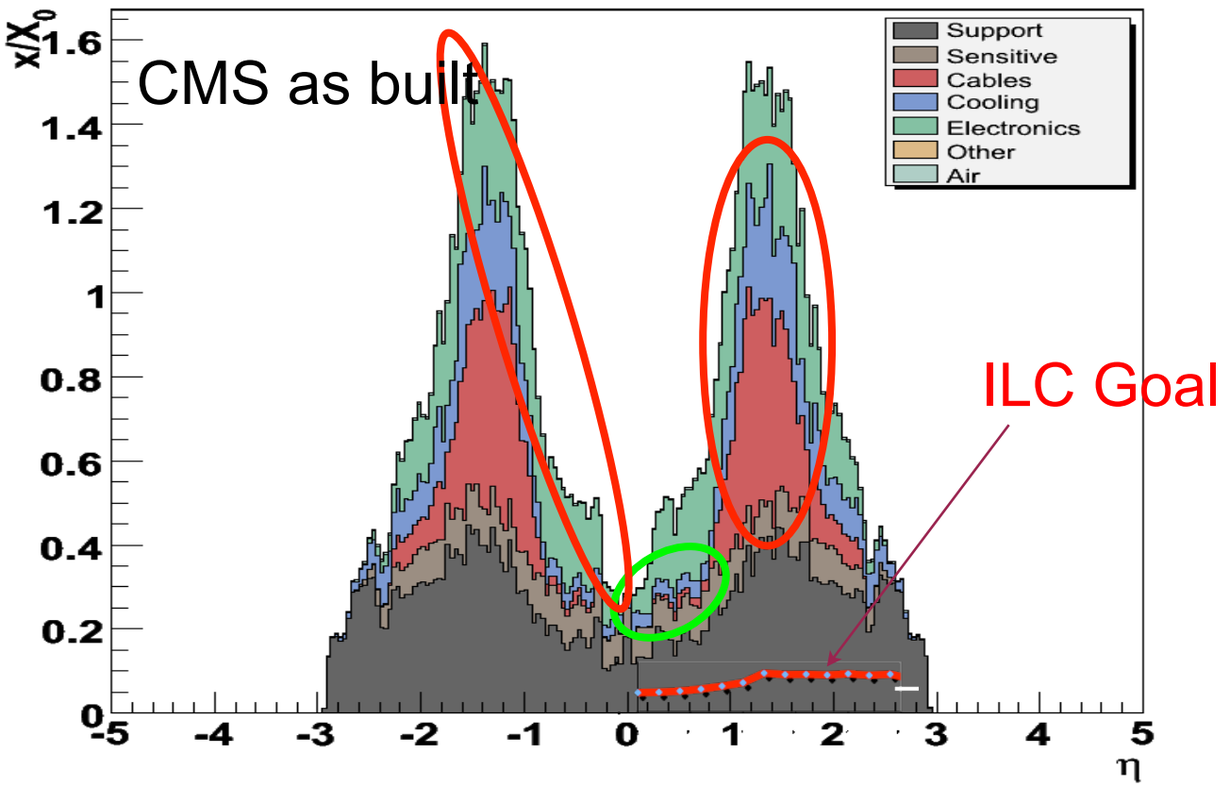
SOI thinned to 6 micon and bonded to 3 mil kapton (MIT-LL)

Some Basics

- A MIP deposits 80 e-hole pairs/micron in silicon
- Charge mobility:
  - Electrons: ≤1400 $cm^2\ V^{-1}s^{-1}$
  - Holes: ≤450 $cm^2\ V^{-1}s^{-1}$
- Noise scales as capacitance
  - Can range from ff in pixels to 10's of pf in strips
  - A multiply-sampled CCD output node can achieve single electron noise
- Noise scales as $(1/\text{rise time})^{1/2}$
- Time resolution ~ (Rise time)x(noise/signal)

Power Consumption

- Limiting Power consumption is crucial for low mass pixelated detectors (CMS Tracker- 17 kAmp)
  - Move electronics off-detector
  - Limit power to allow air cooling
  - Use CO_2 cooling
- There are basic power-speed and detector tradeoffs



	# Pixels / chip	Pixel area [mμ²]	Idig [mA]	Iana [mA]	Power/ chip [mW]	Power/ pixel [μW]	Power density [mW/cm²]
ALICE	8192	21'250	150	300	810	99	466
ATLAS	2880	20'000	35	75	190	67	335
CMS	4160	15'000	32	24	121	29	194
			CMS	no on-chip regulators	87	21	142

(R. Horisberger)

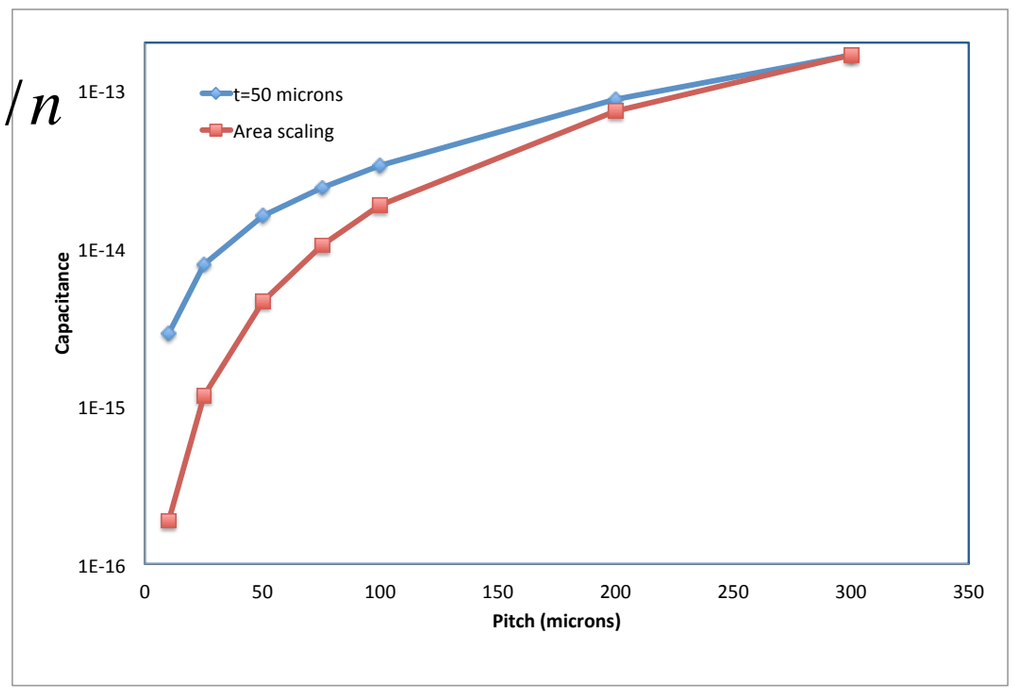
Power and Pixel Size

- Noise scales as C and 1/sqrt[$g_m\tau$], g_m~(qI_d/nkT).
- For a strip or pixel detector for a given noise
  - I ~ C^2, P ~ C^2
  - C ~ (width/pitch) x length (modulo edge effects)
- If divided into n pixels/strip of spacing p x p (ignoring perimeter effects)

$$C_{strip} \cong k\frac{w}{p}l, \quad P_{strip} \propto \left(k\frac{w}{p}l\right)^2$$

$$C_{pixel} \cong k\frac{w}{p}p, \quad P_{n\ pixels} \propto \left(k\frac{w}{p}l\right)^2\frac{p}{l}, \quad P_{n\ pixels} \cong P_{strip}/n$$

where the real factor depends on edge effects, overhead, and non front-end power.



Electronics for Fast Tracking

We clearly would like fast (ns level) time stamping or gating. We also need fine segmentation, low mass, and good resolution. The electronics and sensors also have to be radiation hard

- We will have to pay… but how much?
- The price is power which implies mass
- We also have increased mass for cooling in a radiation environment

  ILC had very aggressive mass goals (0.1%/layer)– but what is really needed for the physics at Project X?

How to build a fast silicon tracker

1. Minimize Collection time
   Collect electrons (μ_e=1350 cm/V*sec, μ_h=1350 cm/V*sec)
2. Fast amplifier
   $T_r \sim 0.35/f_u$, $f_u \sim g_m/(2\pi C_{gs})$, High transistor g_m
3. Good signal/noise
   $\sigma_t \sim T_r/(S/N)$
4. Low noise, high signal
   - $(S/N)^2 \sim Q_s^2(1/(4kT\Delta f)\ (g_m/C_d^2)$, thick detector, short strips
   - $Noise^2 \sim 1/g_m \sim 1/I_d$ – direct power penalty

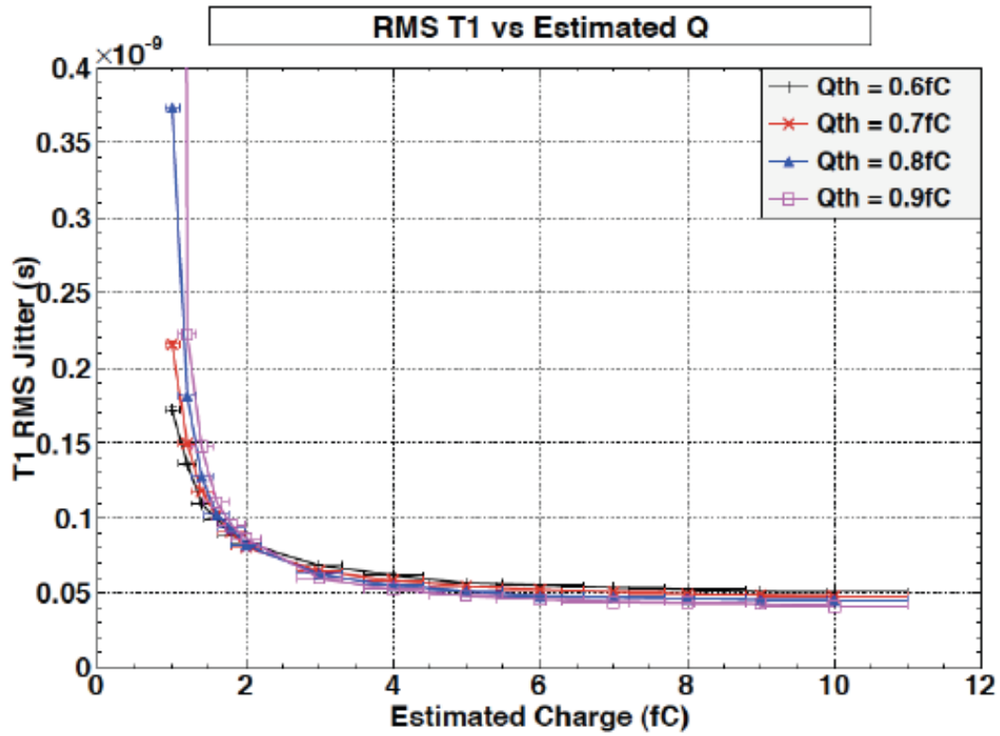
Minimize detector thickness for short collection time
Maximize detector thickness for low C_d, high Q

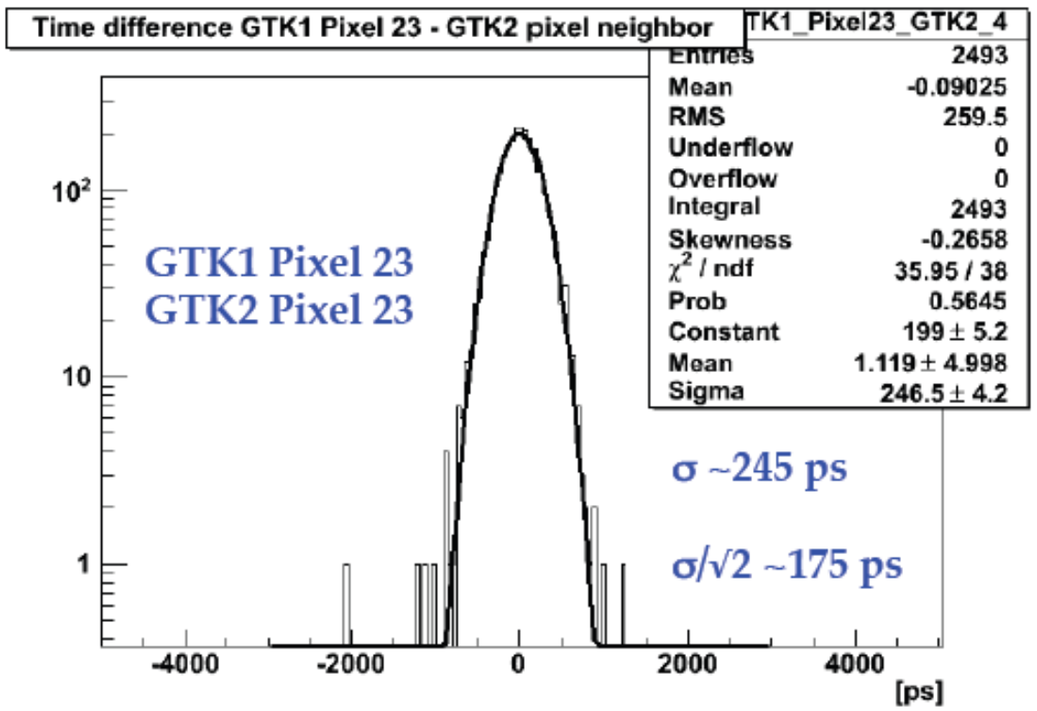
Example – NA62 Gigatracker

Designed for K_L-> πνν decay in flight.

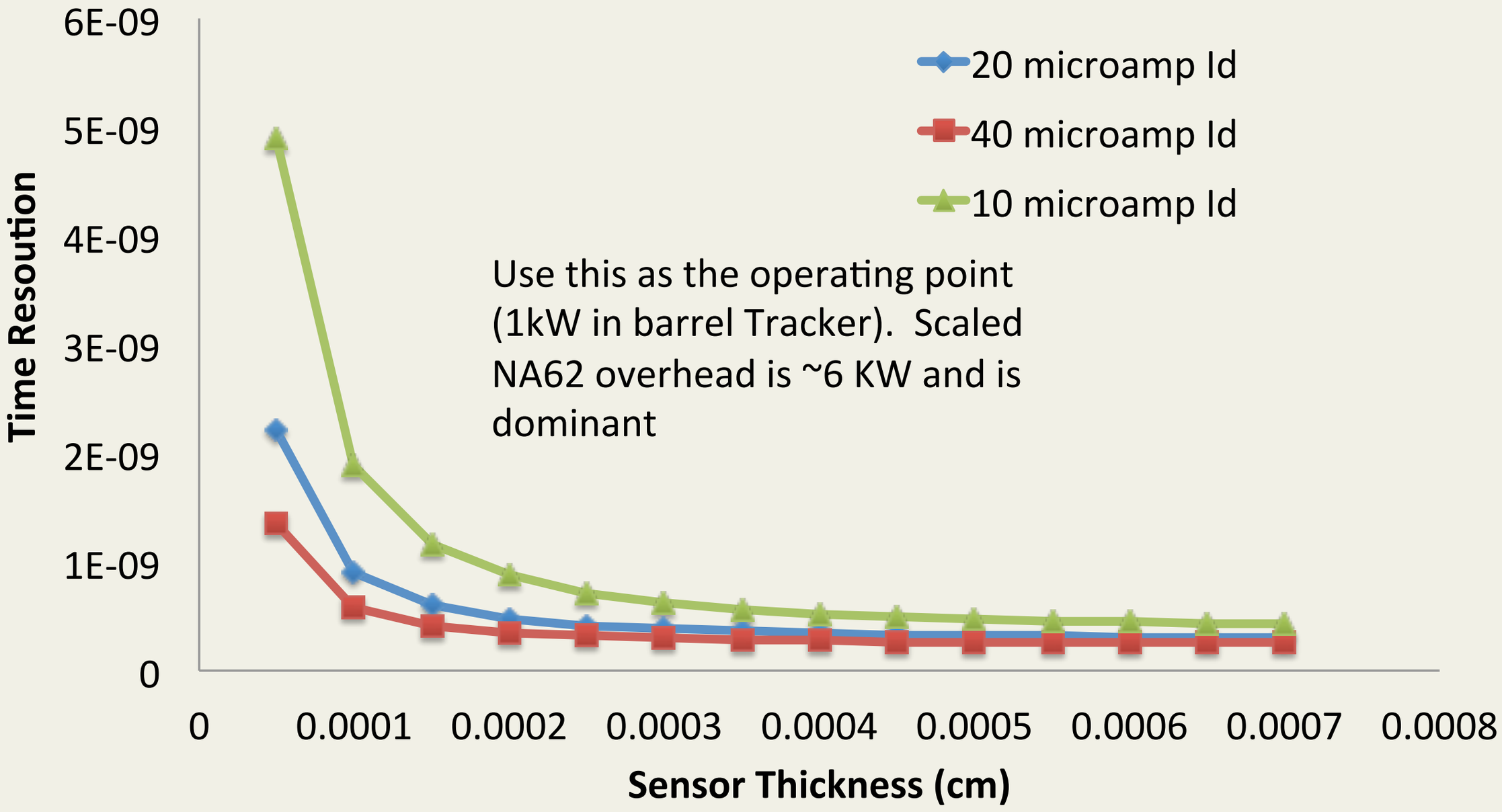
- 800 MHz DC beam
- <200 ps hit timing resolution
- 40 µA front end transistor bias
- 200 micron silicon
- 200 ff detector capacitance

We can scale our models to the NA62 design, changing I_d, C_d, to match pixel size and transistor currents to estimate what we need for nanosecond level resolution





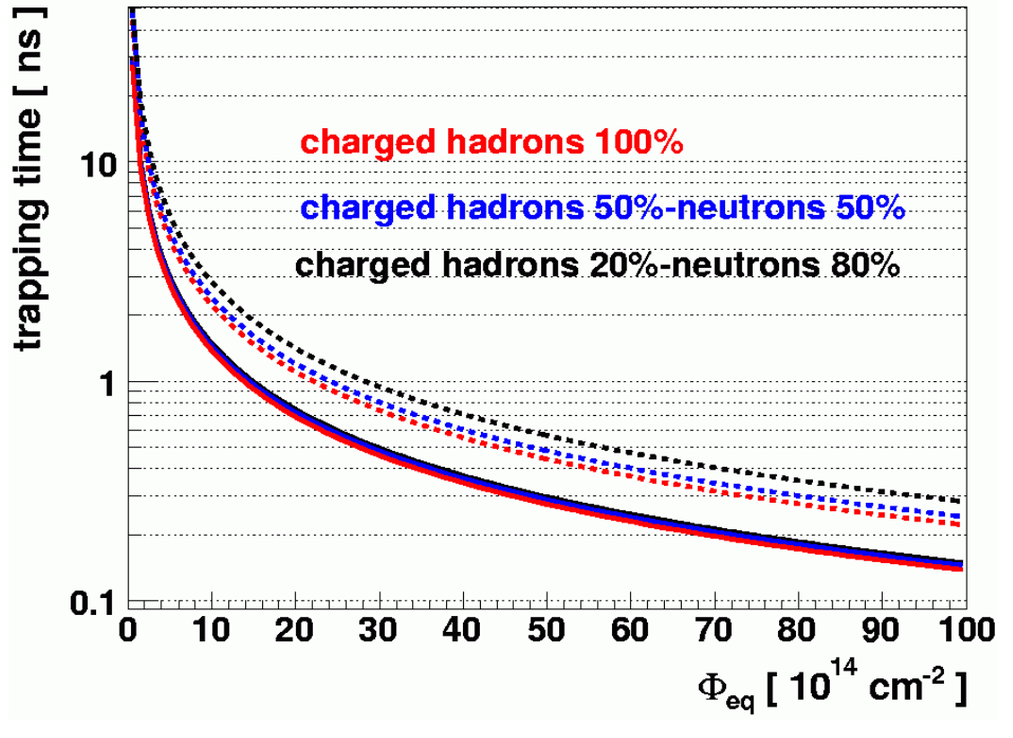
Time Resolution vs Sensor Thickness
1 cm strips, assume charge sharing
(scale from NA62)

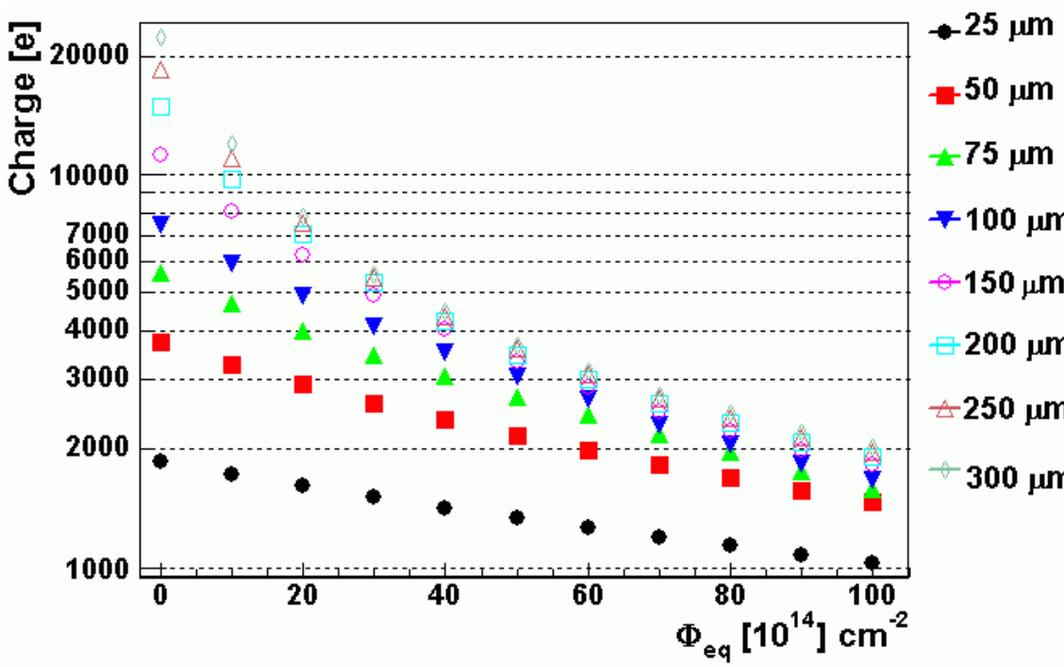


Thinned Detectors and Radiation Tolerance

- Radiation reduces the mean free path of charge carriers in silicon
  - Thinned detectors collect almost as much charge as thicker detectors after irradiation
  - Depletion voltage is much lower (V_d~thickness^2)
  - Leakage current is lower ~ t
- Of course the initial signal is 3-6 times lower …

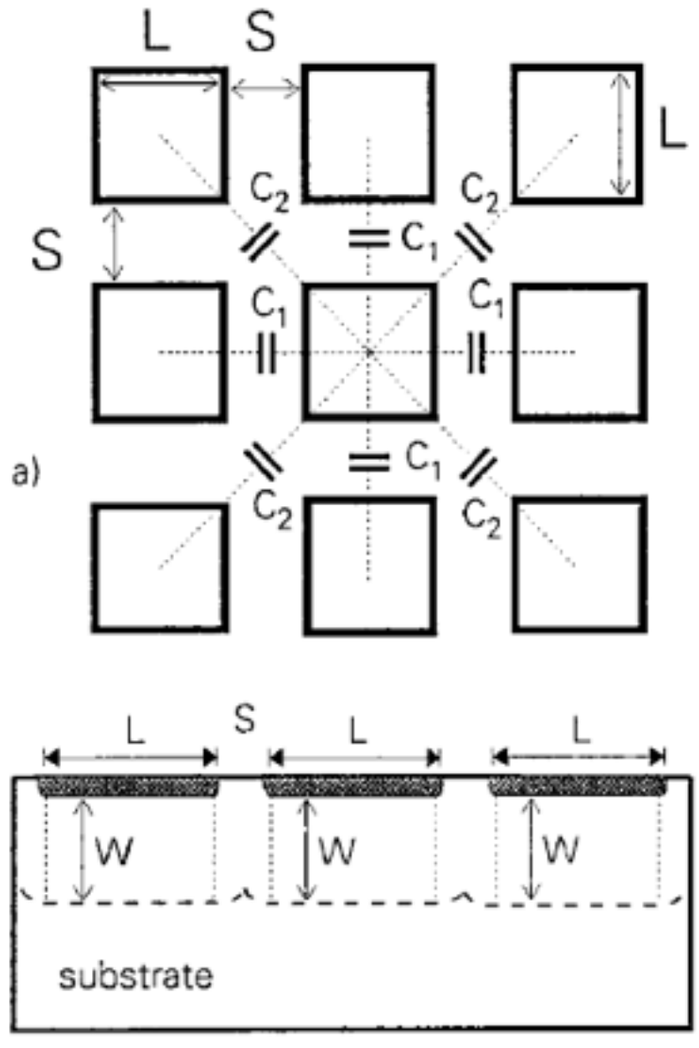
3D detectors (Parker, Kenny) address this problem using deep etching 3D technology





Low Mass Silicon Tracking - Limits

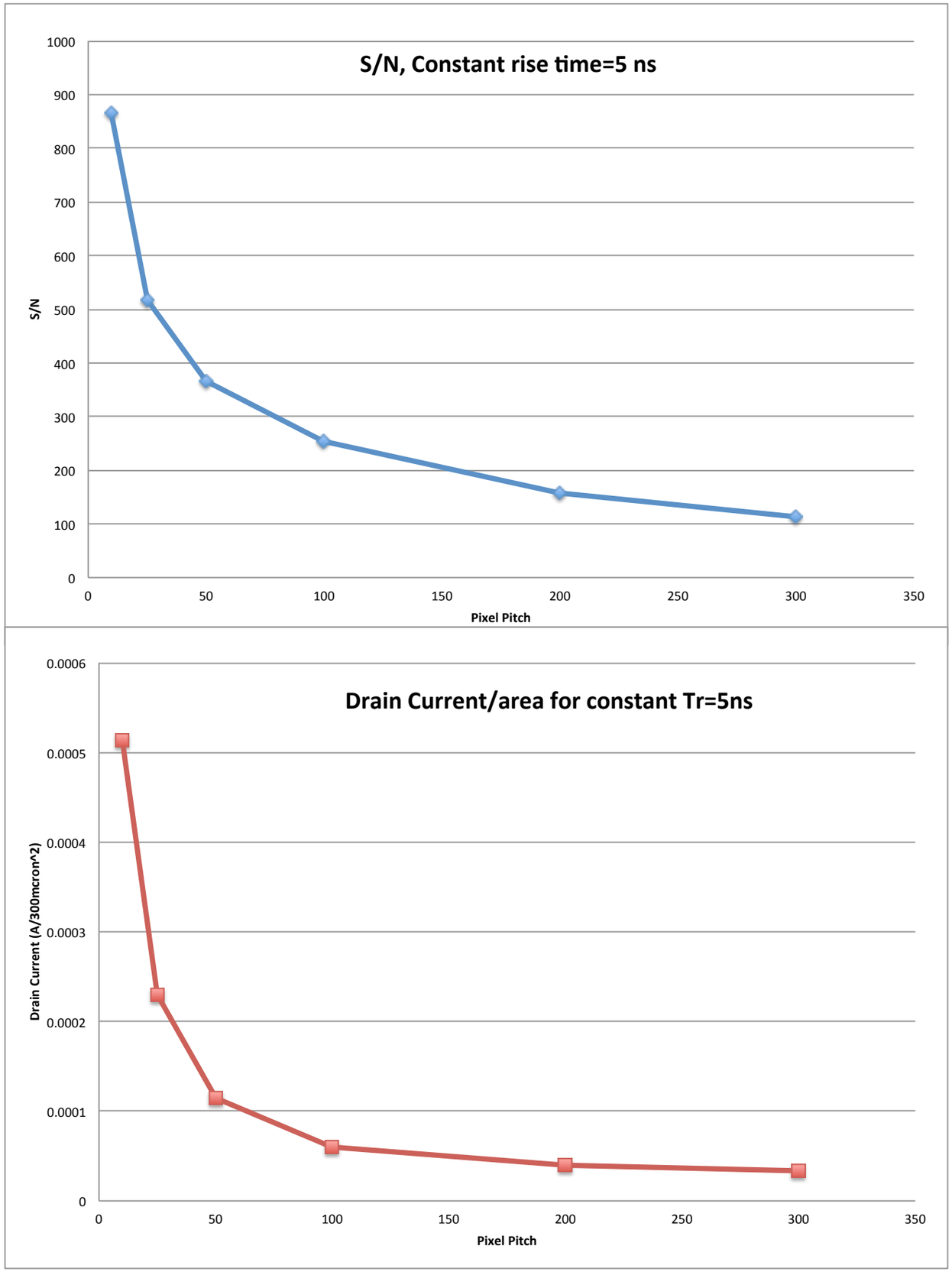
- Signal/noise - Need at least 20:1 ratio.
  - Signal - 80 e/micron
- Noise depends on speed and capacitance
  - Two components to capacitance - neighbor and body ($\varepsilon A/d$)
  - Body capacitance scales with thickness



- Use $(S/N)^2 \sim Q_s^2(1/(4kT\Delta f)\ (g_m/C_d^2)$
- Analytic estimate of pixel cap. from Cerdeira and Estrada

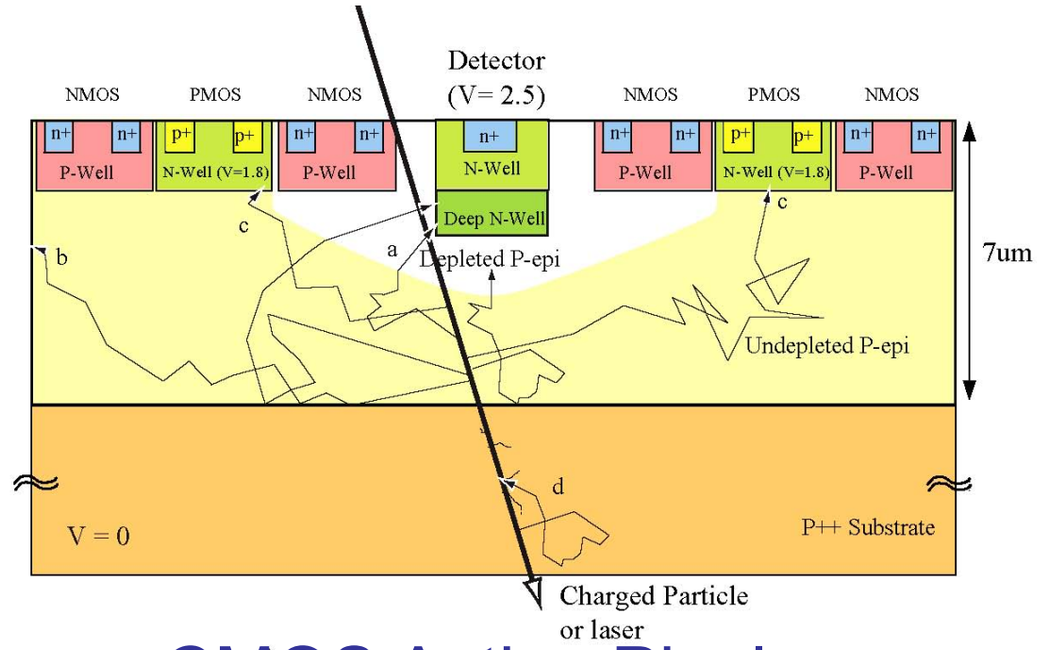
Pixel Pitch Scaling

- Constant rise time - maintain ratio of g_m/C_d
- Constant signal/noise maintain ratio Sqrt(g_m)/C_d
- Constant time resolution- maintain ratio t_r/(S/N) ~sqrt(g_m) - just depends on drain current

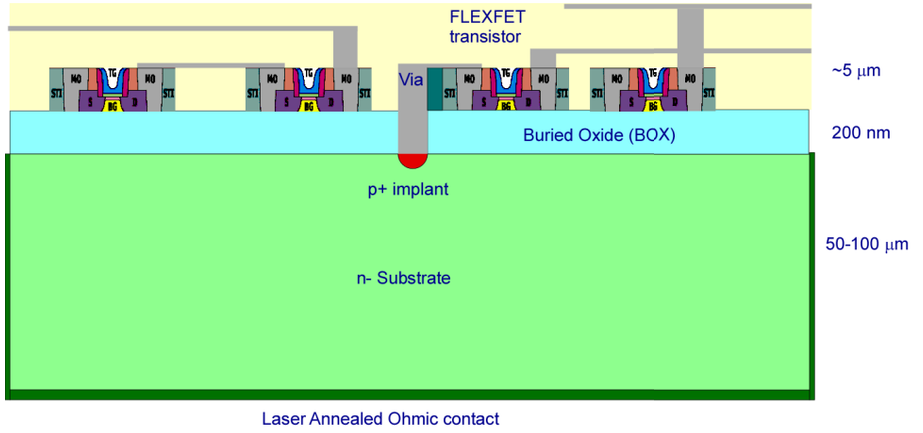


Low Mass Silicon R&D

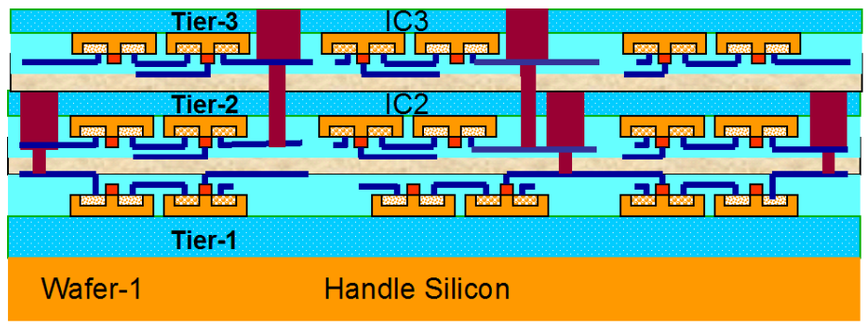
- We know we can get good S/N with thin, pixelated detectors - what technologies are available to achieve this?
- Much R&D related to ILC which requires <.1% Rl per layer
- Too much to go over details in a brief talk - but there are many choices. I will concentrate on FNAL work



CMOS Active Pixels



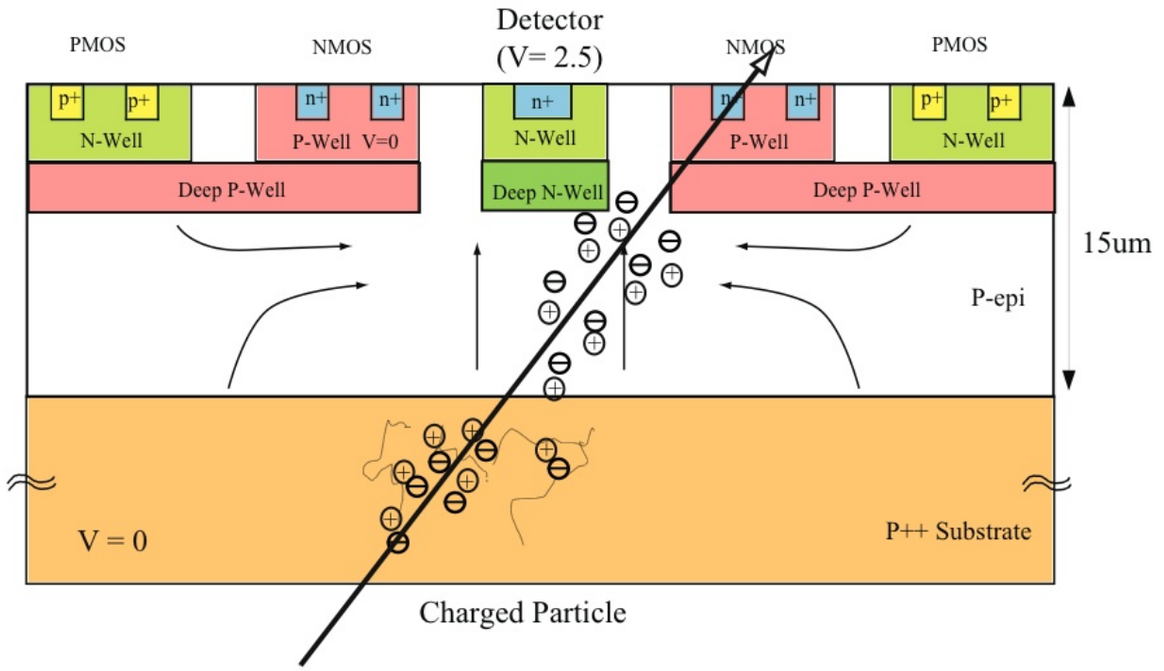
SOI



3D

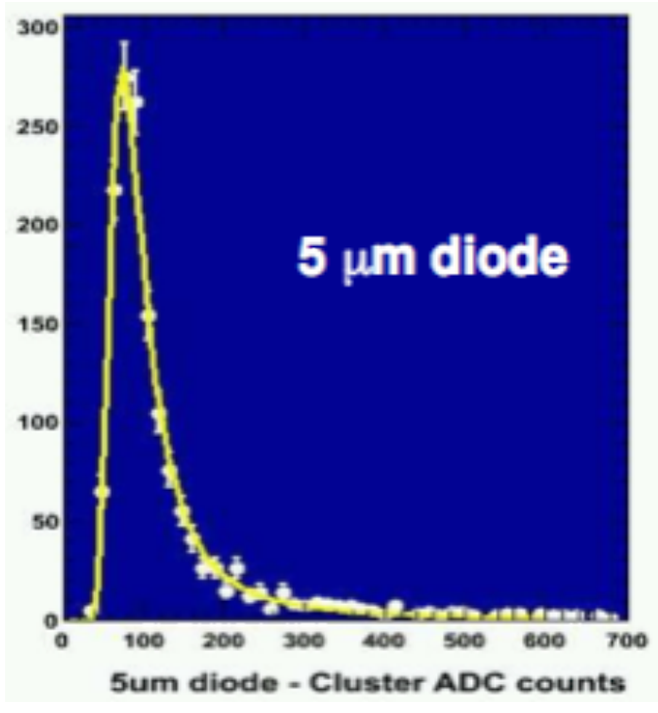
MAPS

- Uses “standard” CMOS processes with charge collection in a thin (5-20 micron) epitaxial layer



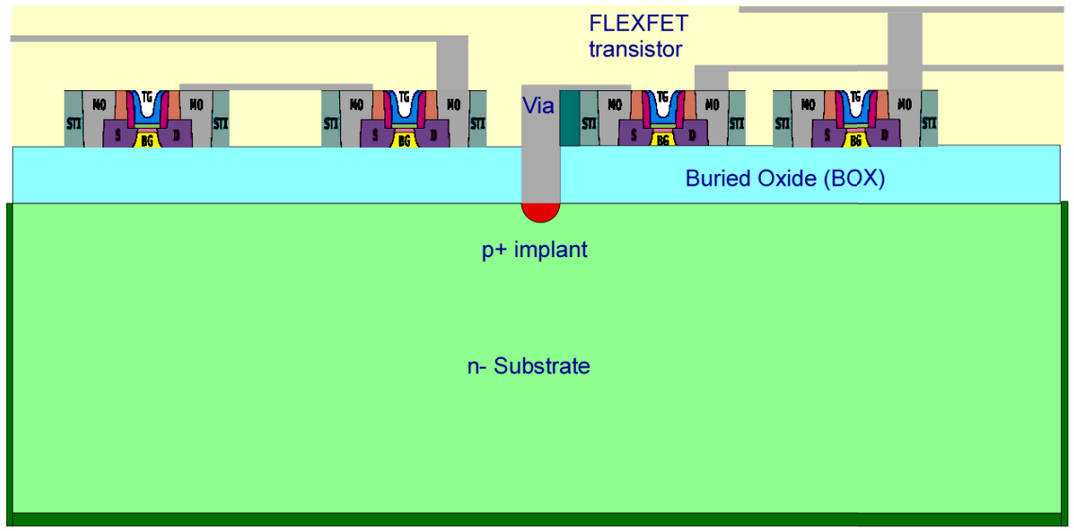
- Charge collection by diffusion - slow (100 ns)
  - Alternate “depleted” processes being explored - can have large leakage currents
- Parasitic charge collection in nmos transistors
  - Enclose structures in multiple wells
  - 3D integration
- Relatively easy thinning due to the thin epitaxial layer
- Used for STAR vertex layer

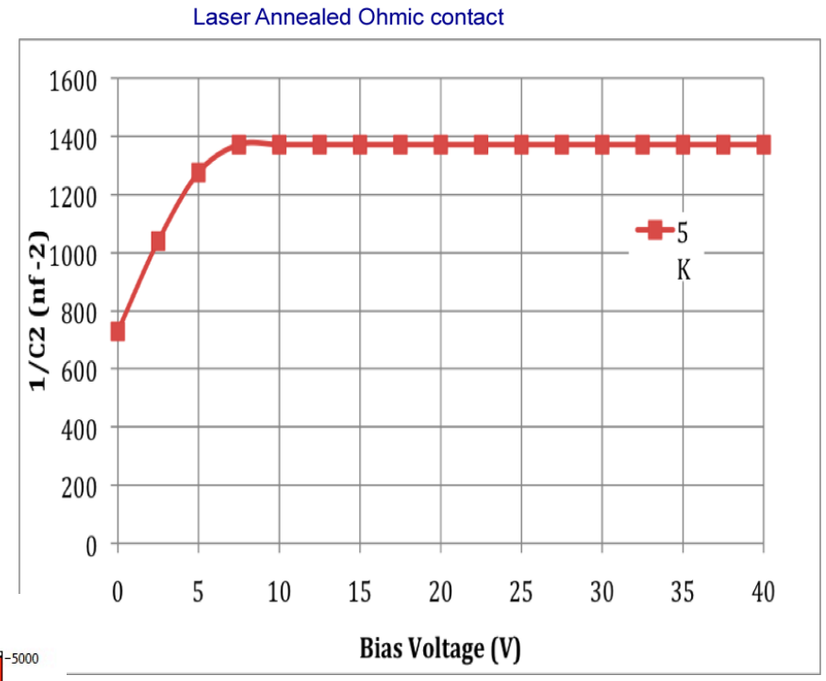
LBL 5 micron pitch,
14 micron epitaxial

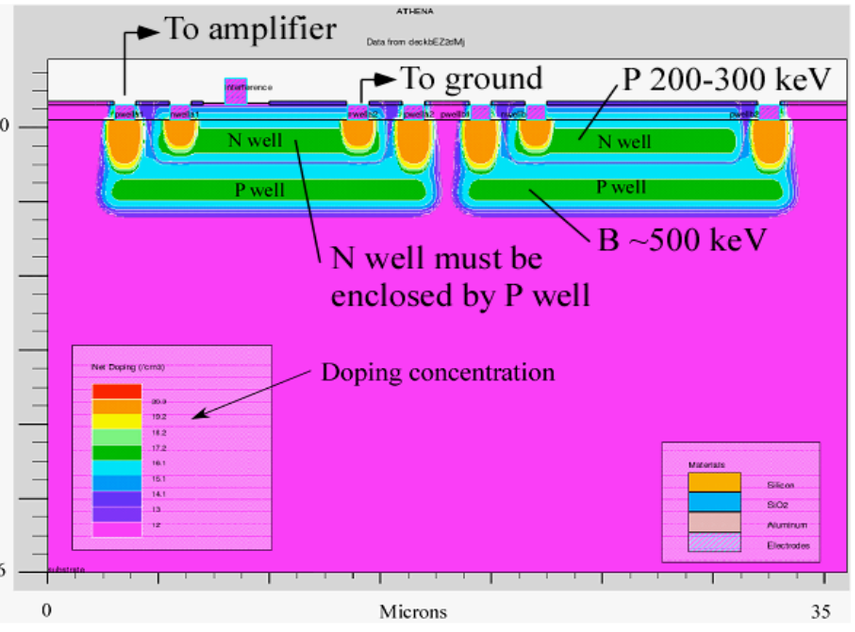


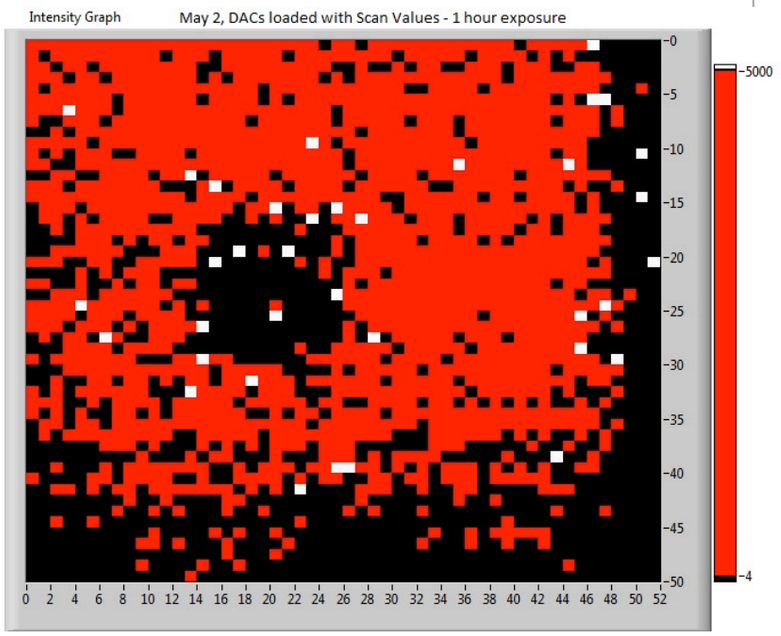
Silicon-on-Insulator

- Uses the “handle wafer” of an SOI stack
  - High resistivity silicon, fast
  - Transistor affected by sensor bias “backgate”
- Technologies explored by FNAL with KEK, American Semiconductor
  - Thinned to 50 microns
  - Laser anneal backside contact
  - Implants to avoid backgate
  - MAMBO first complex in-pixel design
- Standard SOI is not very rad hard, but ASI FLEXFET should be









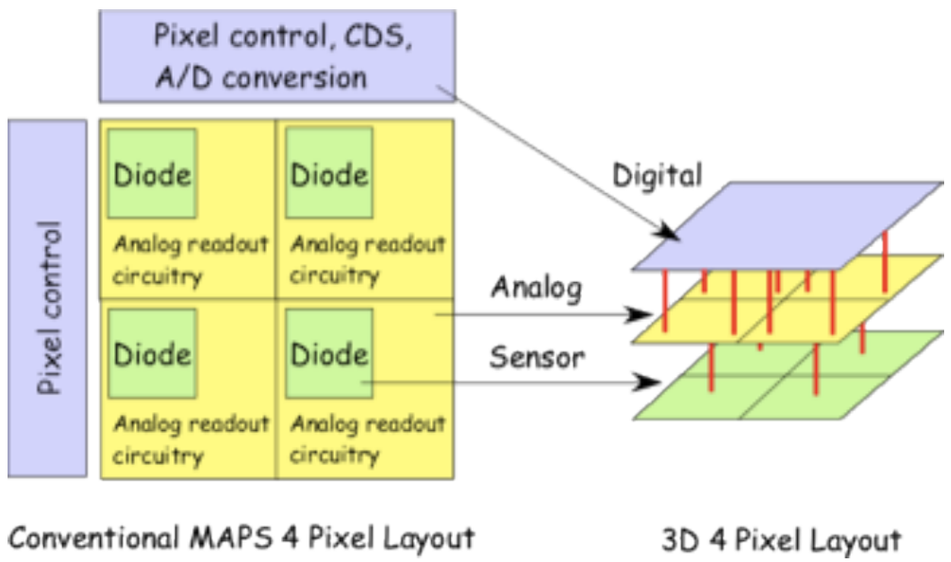
3D Electronics

3D circuits are a major thrust for the IC industry

- They allow bonding of multiple layers of ICs in an single stack - increasing speed, reducing inductance and capacitance
- New technologies for wafer bonding, thinning, interconnect

They have transformative applications in HEP, and will change the way we design silicon tracking

- No fine pitch bump bonds
- Lower capacitance
- Integrated sensors and electronics



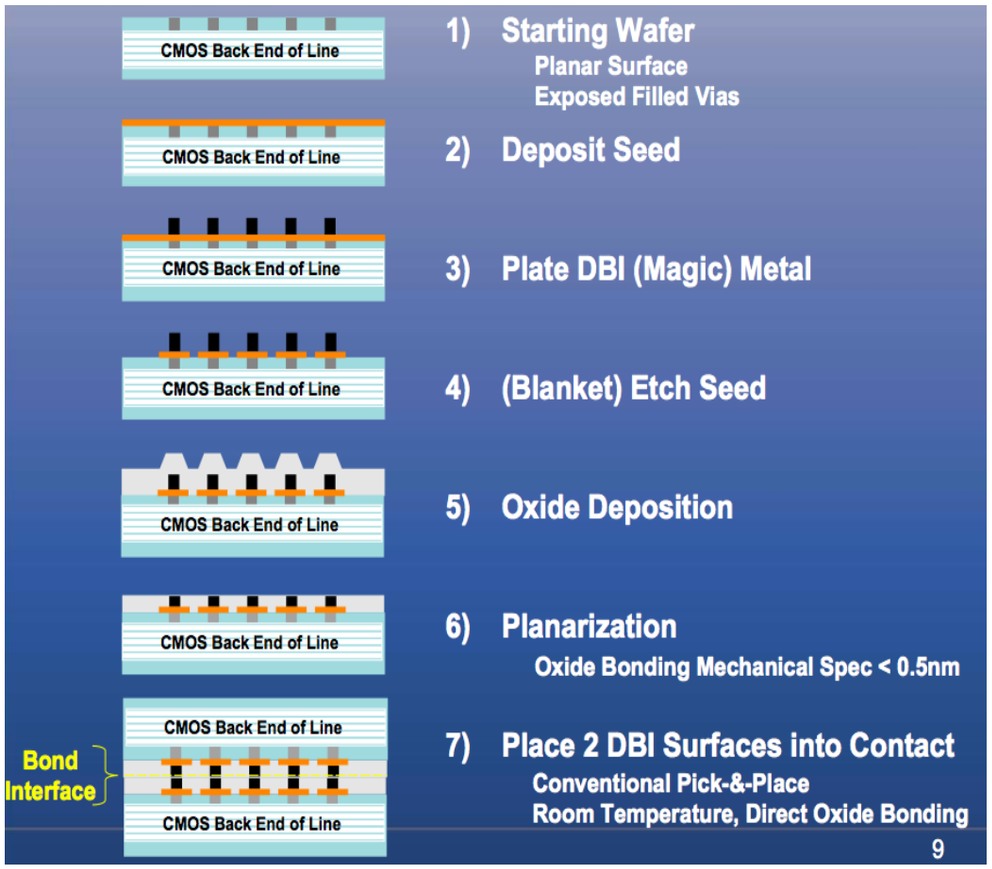
3D for HEP

Why is 3D technology important for HEP?

- It enables intimate interconnection between sensors and readout circuits
  - Subpixel readout and control of SiPMs
- It enables unique functionality
  - Digital/analog/ and data comm. tiers
  - Micro/macro pixel designs which can provide high resolution with minimal circuitry
- Wafer thinning enables low mass, high resolution sensors
- Bonding technologies enable very fine pitch, high resolution pixelated devices
- Commercialization of 3D can reduce costs for large areas
- Unique circuit/sensor topologies (CMS track trigger)

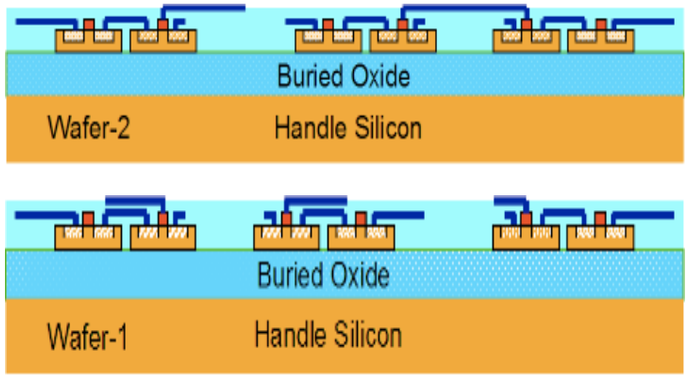
Processes Explored

Ziptronix Oxide Bonding

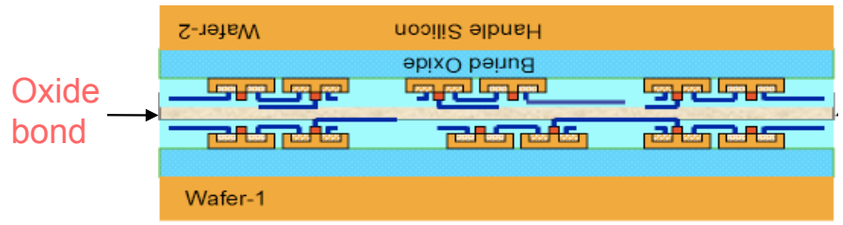


MIT-LL Oxide wafer bonding

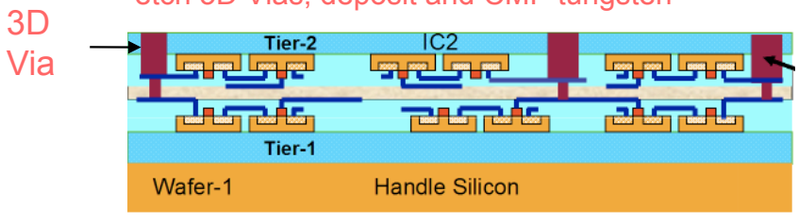
1) Fabricate individual tiers

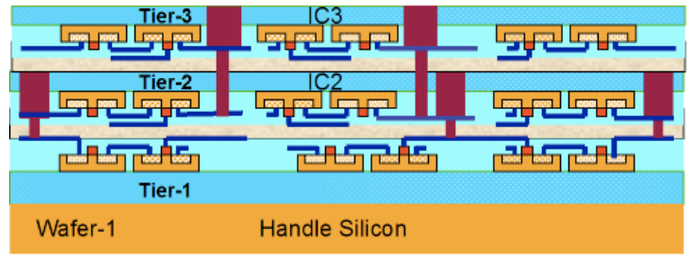


2) Invert, align, and bond wafer 2 to wafer 1

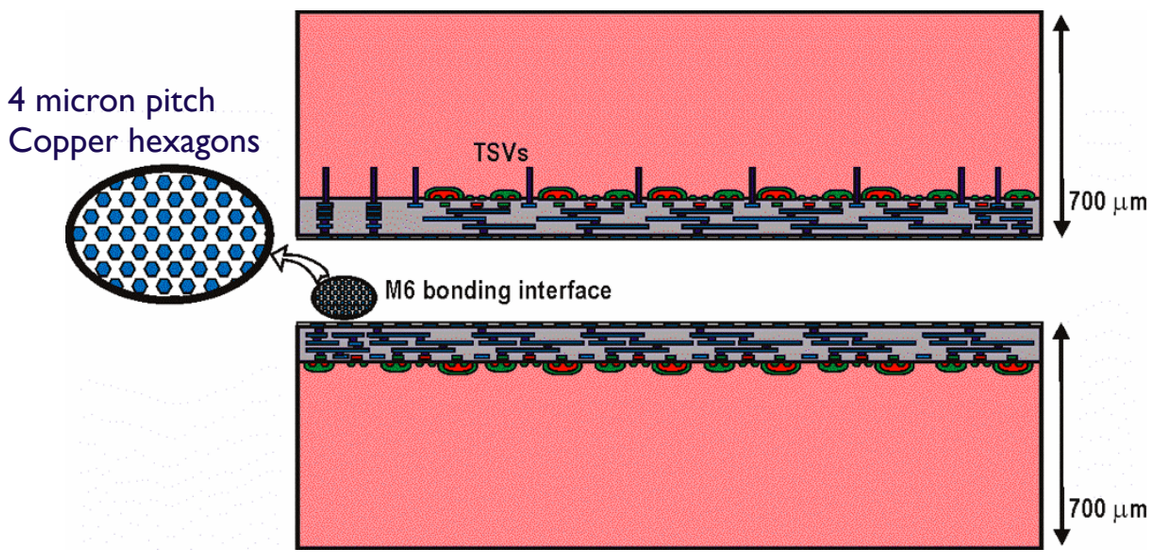


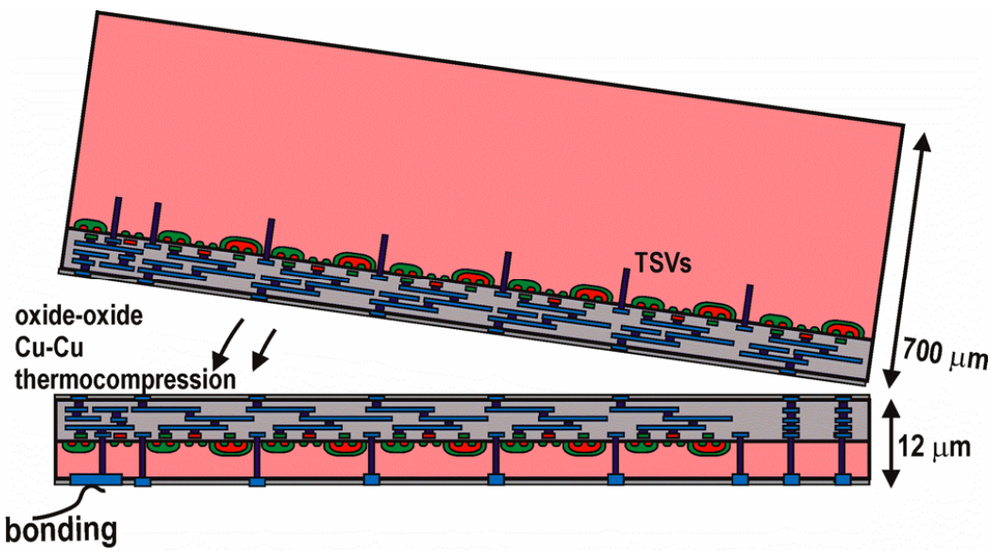
3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten





Tezzaron cu-cu bonding



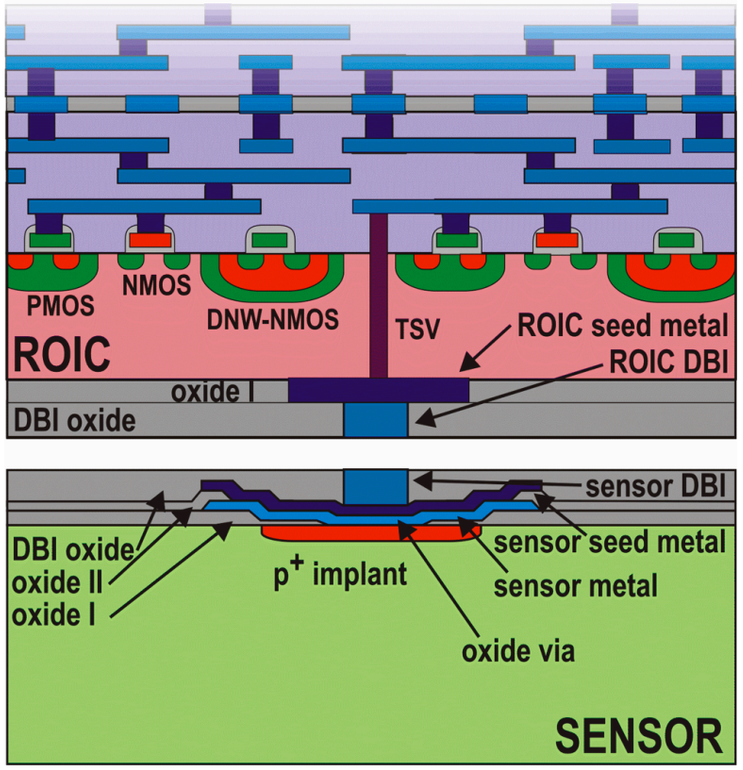


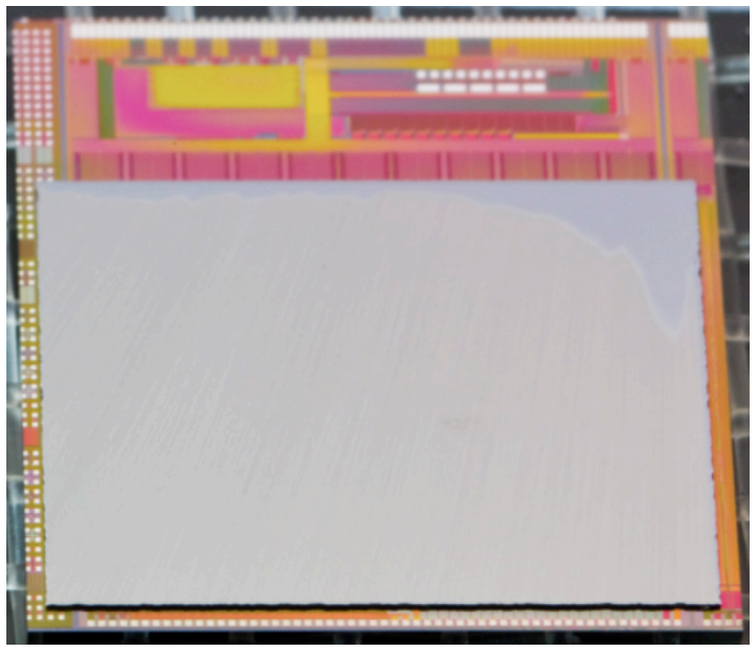
3D Integration by Oxide Bonding

Ziptronix Direct Bonded Interconnect (DBI) based on formation of oxide bonds between activated SiO2 surfaces with integrated metal

- Silicon oxide/oxide inital bond at room temp. (strengthens with 350 deg cure)
- Replaces bump bonding
- Chip to wafer or wafer to wafer process
- Creates a solid piece of material that allows bonded wafers to be aggressively thinned
- ROICs can be placed onto sensor wafers with 10 µm gaps - full coverage detector planes
- ROICs can be placed with automated pick and place machines before thermal processing - much simpler than the thermal cycle needed by solder bumps

Text

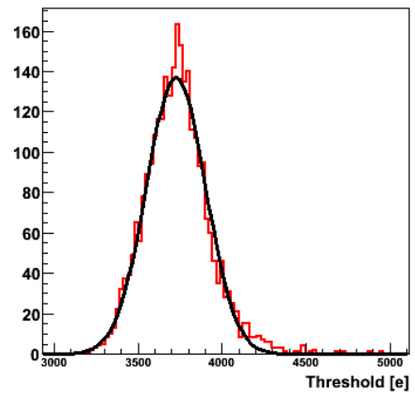


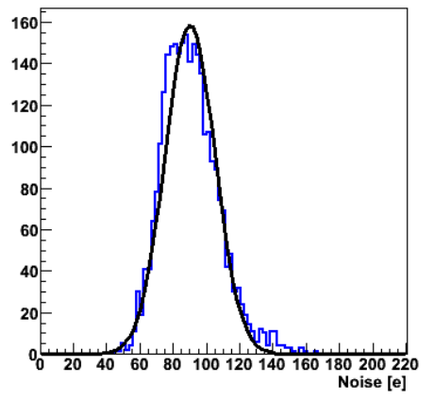


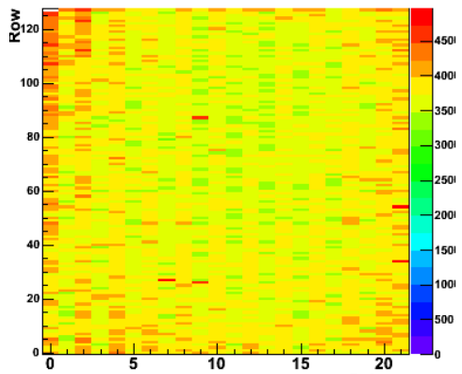
- BTeV FPiX 2.1 ROICs - 22 x 128 array of 50 x 400 micron pixels. - 8” wafers
- MIT - LL 300 micron thick sensor wafers which had a matching pixel layout - 6” wafers
- Sensor “chips” were bonded to 8” ROIC wafers, then thinned to 100 microns

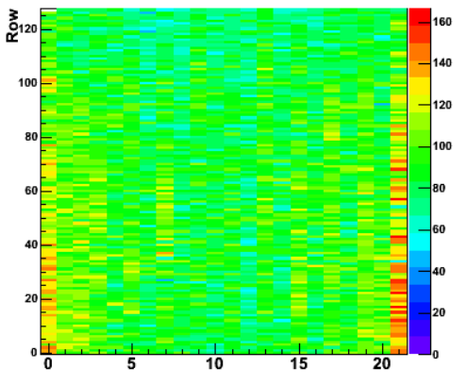
Device Tests

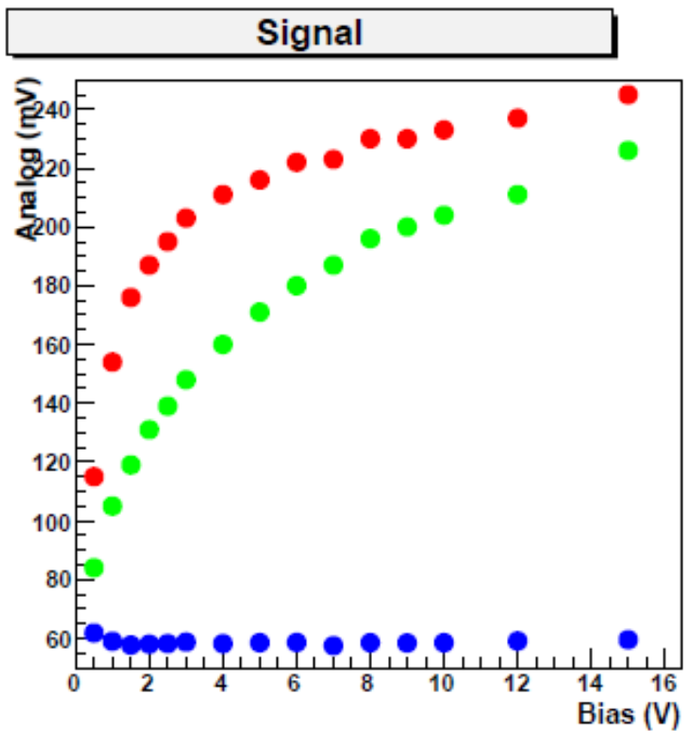
- 1064 nm laser used to test response of edge channels with analog outputs
  - Vdepl ~ 8V
  - Low capacitance associated with interconnect
  - No evidence of digital to analog crosstalk
  - Good overall performance - all channels connected on die without bond voids.
  - Void rate ~ 4/21(wafer1), 12/25 (wafer 2)

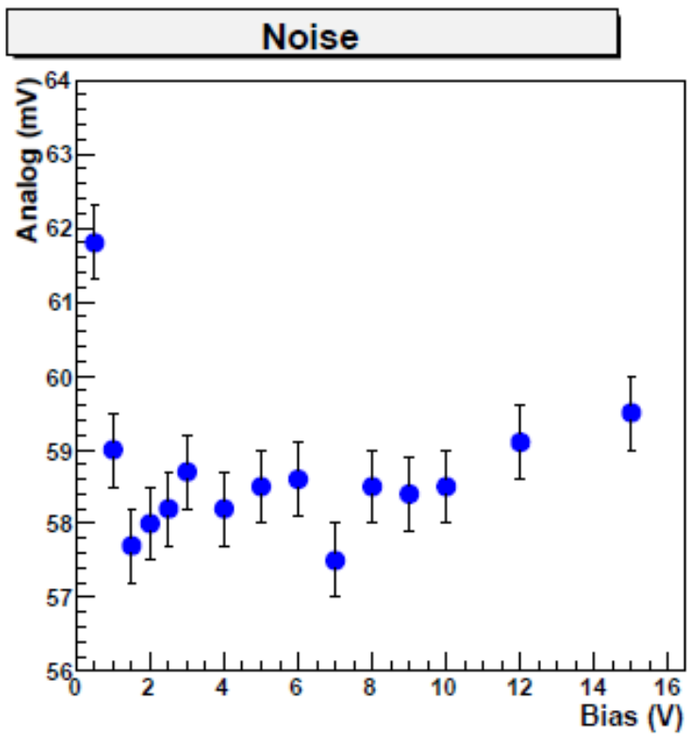


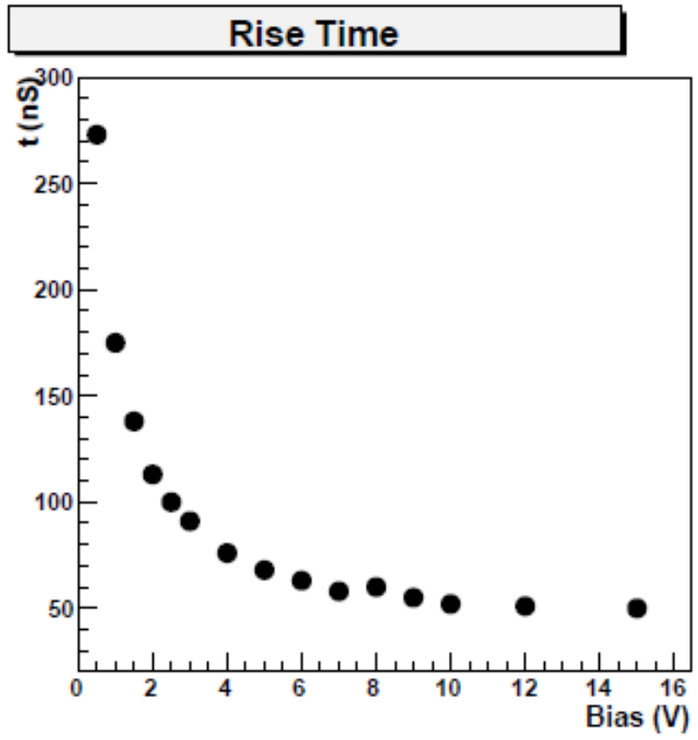








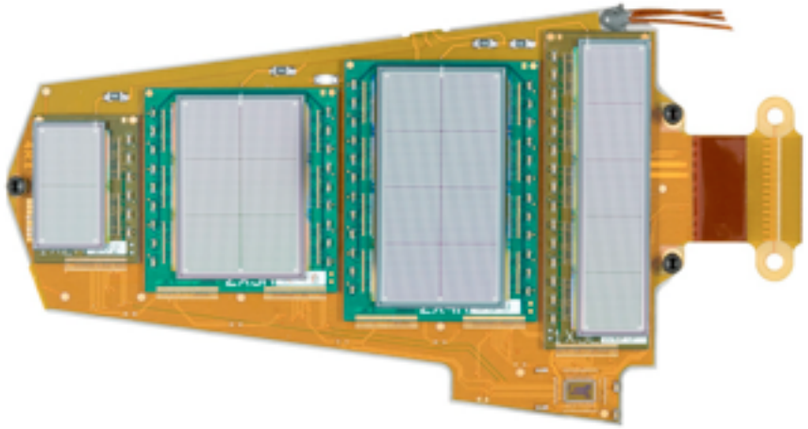




Large Area Arrays

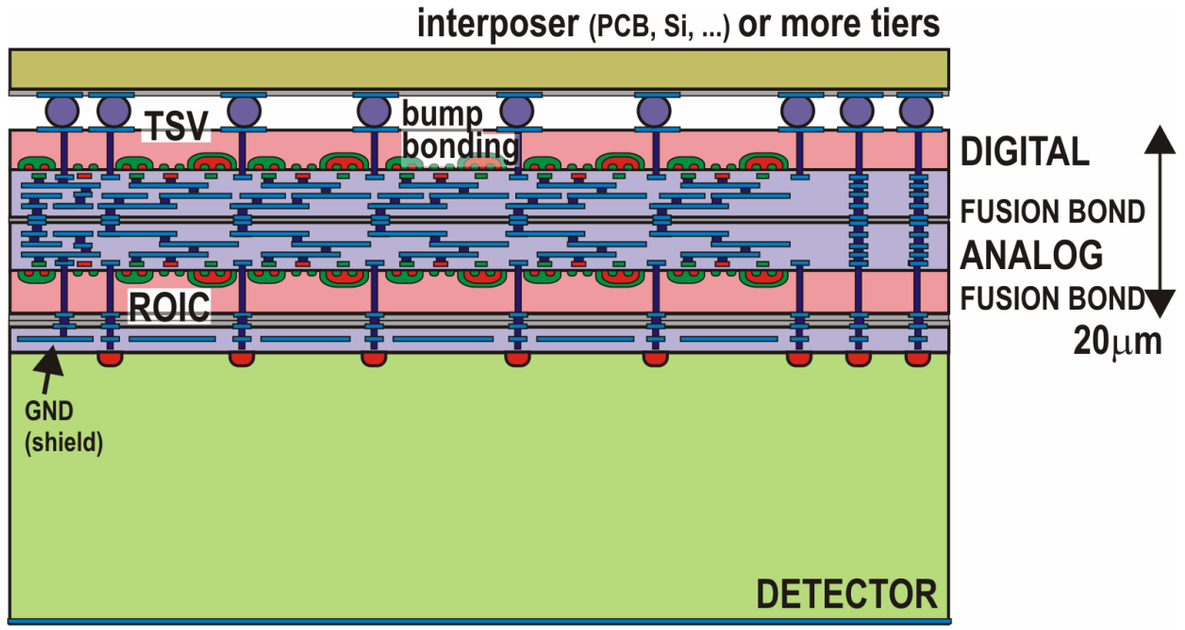
The Problem: Build large area arrays (100s of meter^2)of highly pixelated detectors with minimal dead area and reasonable cost

- Current pixel detectors have dead areas arising from:
  - Edge effects due to cut edge damage
  - Wirebond connections for readout chips (ROICs)
- A possible solution:
  - 3D #1 - Active edge sensors remove dead area at the edges
  - 3D #2 - 3D or vertically integrated electronics provide a backside path for extraction of signals



CMS forward pixel plaquette

The goal of 2x3D work is to combine active edge technology with 3D electronics and oxide bonding with through-silicon-vias to produce fully active tiles.

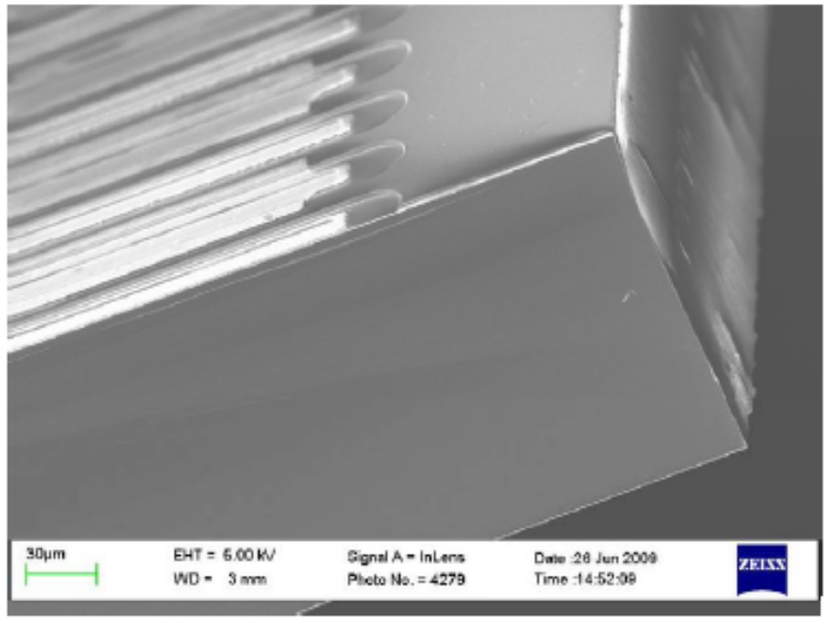


- Driven by CMS track trigger needs (100's of m^2 of 3D pixelated sensors)
- These tiles can be used to build large area pixelated arrays with good yield and low cost because the only bump bonds are large pitch backside interconnects.
- Fine pitch bonds to the sensor are made using wafer to wafer oxide bonding
- The SOI-based technology can provide very thin sensors

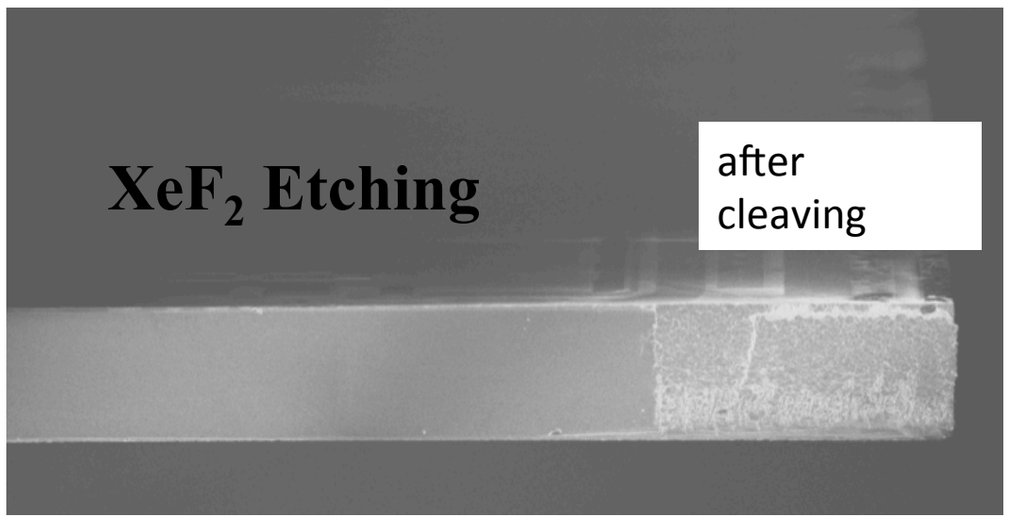
Active Edge Sensors

An outgrowth of 3D detector development by Sherwood Parker and collaborators

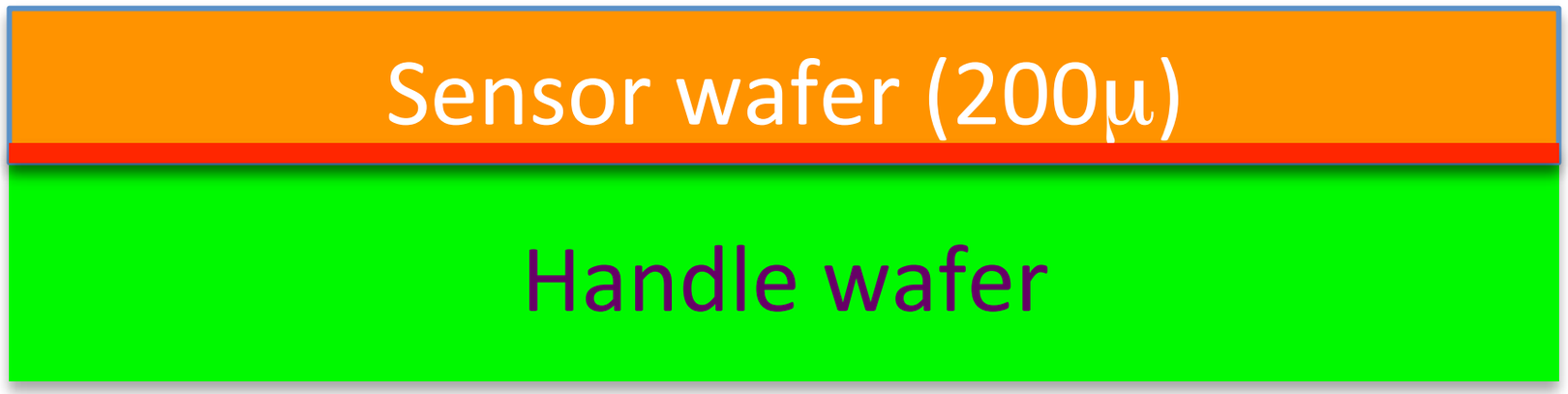
- Deep reactive ion etch of silicon to create a nearly vertical trench with smooth edges avoids charge generation centers
- Filled with doped polysilicon or implanted and annealed to create a “backside” electrode
- UC Santa Cruz/Naval Research Lab is exploring an alternate process involving cleaving and atomic layer deposition



VTT Active Edge Sensor

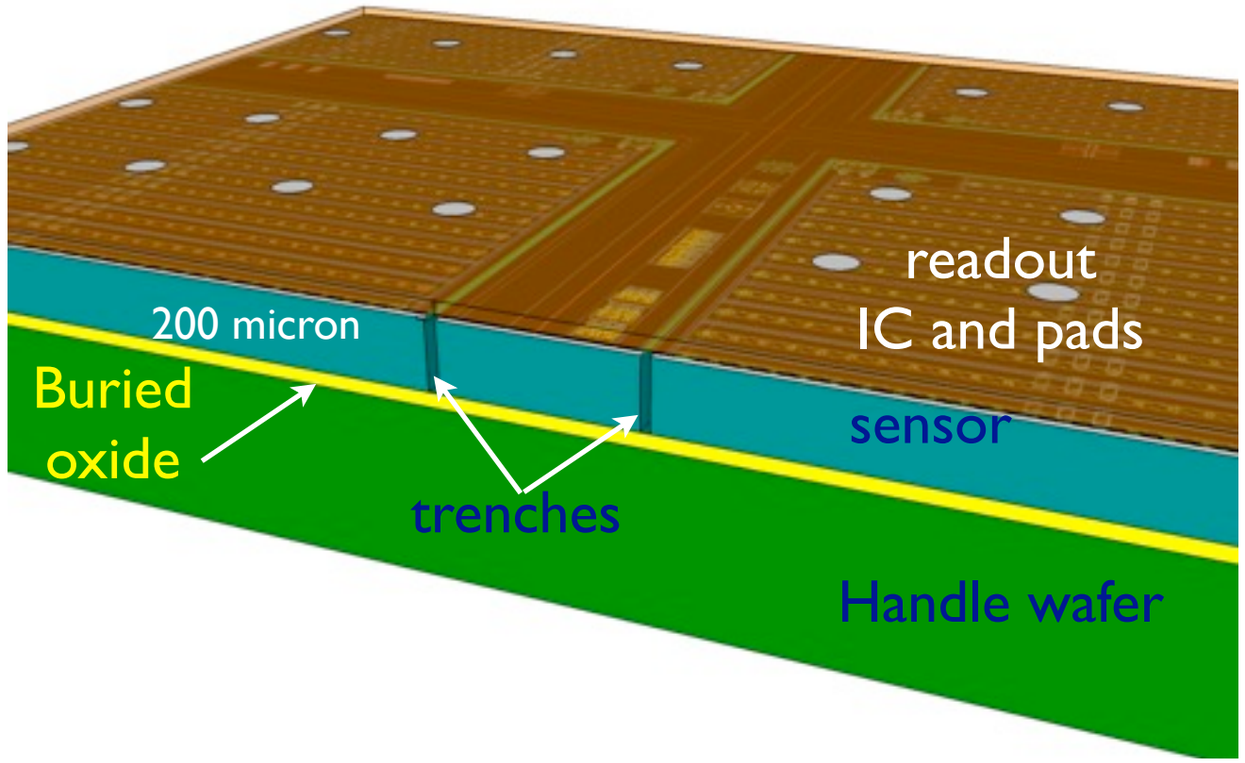


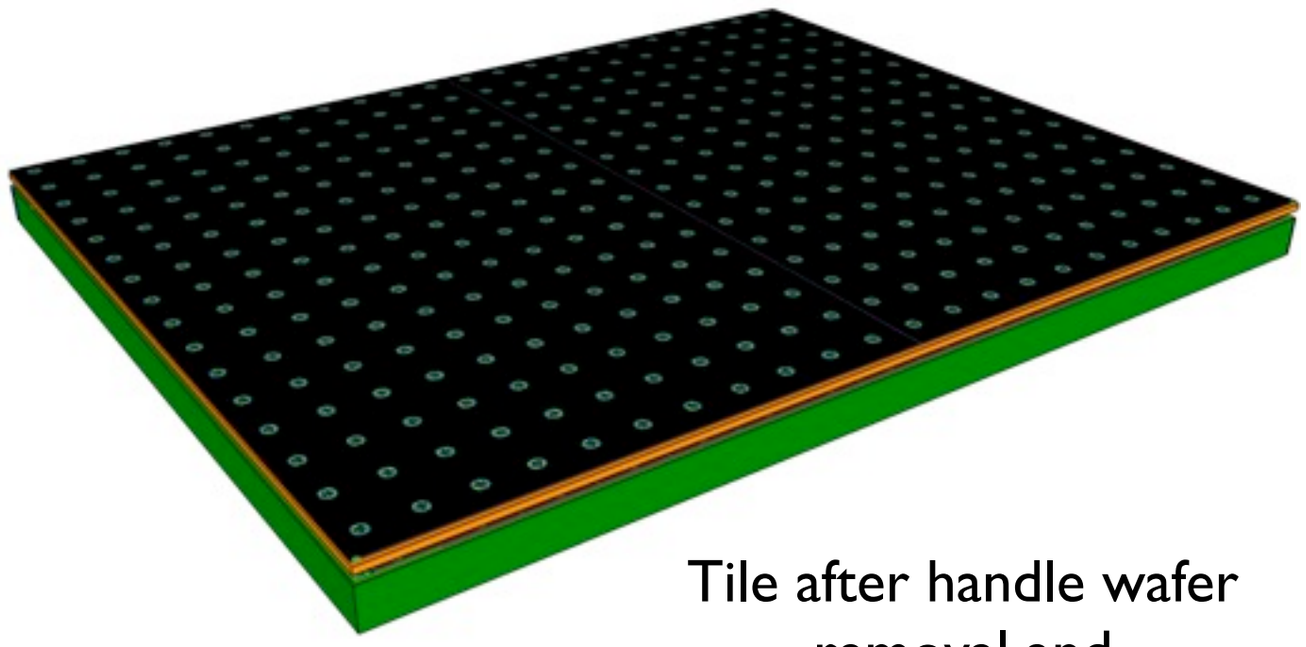
3D Active Edge Fabrication Process



Active edge assembly

- As a final step the polysilicon in the trenches and the handle wafer have to be removed - this will be done at Stanford in collaboration with SLAC
- There are no trenches on the edge reticules to allow test of the UCSC/ NRL process



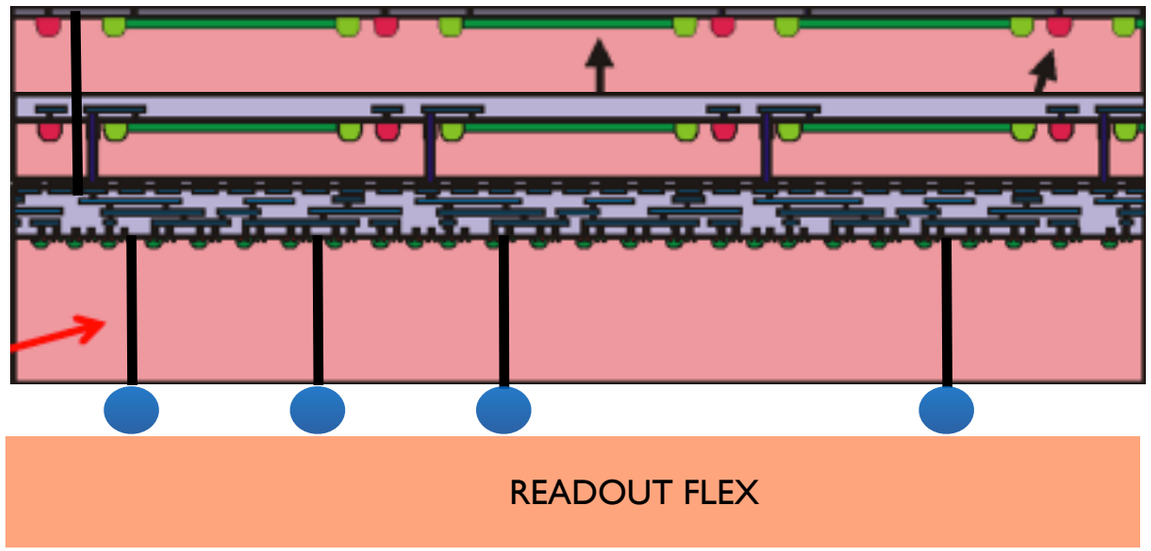


Tile after handle wafer removal and singulation

Workshop level thoughts

- **Much of the power is devoted to biasing the front-end transistor**
- **We can avoid this using avalanche effects in silicon (like gas)**
- **SIPMs could do this if the singles rates were not so high**
  - **More than enough primary electrons in an SIPM thinned to 10-20 microns**
  - **High "single photon" noise rates**
    - **Ask for multiple hits**
    - **Use 3D integration to mate 2 SiPMs and ask for coincidence**
      - **Response could be very fast - <100 ps since all capacitances are low**
      - **Subpixel hit resolution ~15 microns**

Ask for coincidence between top macropixel (~mm) and bottom micropixels readout with micropixel granularity



Conclusions

- Candidate technologies exist for precise, low mass silicon tracking systems.
- Details matter
  - What resolution?
  - How fast?
  - How much power?
    - Mass constraints
  - What area?

Signal/Noise Estimates